Title: VCO-based ADCs for direct digitization of ExG signals

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Abstract: Wearable health sensors can disrupt the healthcare system by providing health professionals with continuous, long-term, high-accuracy physiological data of patients, allowing for more accurate and personalized care. These wearable biopotential sensors have application-specific challenges regarding dynamic range, input impedance, and power consumption. The dynamic range must be wide (>90 dB) to process the small signals of interest (<1 mV) in the presence of large common-mode and differential-mode artifacts (>100 mV). The input impedance of the analog front-end must be high to interface with the high source impedance of small dry electrodes typically used in wearable applications. All this while consuming very low power and allowing on-chip digital processing to compress and secure patient data. This pushes the technology choice toward digital-friendly, deep submicron nodes, where designing such a high-performance analog front-end is challenging. To address these challenges, time-based digitization paradigms leveraging voltage-controlled oscillators (VCOs) have been explored to allow for more digital-friendly analog-to-digital conversion implementations. This talk will describe two such designs.

The first design addresses the non-linearity of VCO-based ADC architectures with a mismatch resilient, multiphase quantizer, a gated-inverted-ring oscillator (GIRO), achieving >110-dB spurious free dynamic range (SFDR). Leveraging the time-domain encoding of the first integrator, the ADC's power is dynamically scaled with the input amplitude enabling up to 35% power savings in the absence of motion artifacts or interference. An auxiliary input-impedance booster increases the ADC's input impedance to 50 MΩ across the entire bandwidth. Fabricated in a 65-nm CMOS process, this ADC achieves 92.3-dB SNDR in a 1 kHz BW while consuming 5.8 µW for a 174.7 dB Schreier figure-of-merit (FoM).

The second design presents a 3rd-order VCO-based ADC that leverages pseudo-virtual ground (PVG) feedforwarding (FF), linearizing the VCOs and enabling higher-order noise-shaping with a single feedback DAC. This technique leads to a power-efficient ADC implementation with a wide dynamic range. The ADC is fabricated in a 65 nm process and achieves 92.1 dB SNDR in a 2.5 kHz bandwidth. This results in a state-of-the-art 179.6 dB FoM amongst previously published VCO-based ADCs. The PVG FF technique allows the ADC to attain extremely high linearity, 123-dB peak SFDR, with a wide 1.8 V_{pp} differential input range. The ADC maintains performance with up to 200-mV variation on the 0.8 V supply and across temperatures from 0 to 70 °C.

Author / Presenter BIO:

- Drew A. Hall received a B.S. degree in computer engineering with honors from the University of Nevada, Las Vegas in 2005, and M.S. and Ph.D. degrees in electrical engineering from Stanford University in 2008 and 2012, respectively.
- From 2011 to 2013, he was a Research Scientist in the Integrated Biosensors Laboratory at Intel Corporation.
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- Dr. Hall is an associate editor for the IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) and the IEEE Solid-State Circuits Letters (SSC-L). He is also on the technical program committees of the IEEE Solid-State Circuits Conference (ISSCC) and the IEEE Custom Integrated Circuits Conference (CICC).