**Title**: Pushing the limits of KT/C in Sigma Delta Modulators

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**Abstract**: Thermal noise, which is sampled and aliases in-band in discrete time systems, limits the achievable performance of a noise-shaping ADC. While the performance of such ADCs has advanced significantly over the last 20 years, as quantified by the Schreier Figure of Merit, the theoretical limit of 192 dB continues to stand. Over that period, we have seen the envelope of ADC performance advance from a Schreier FoM of 163 dB 20 years ago, to 185 dB today, with a rate of advance corresponding to ADC performance doubling every 1.6 years. However, this rate of advancement has started to slow in recent years. This work will review some of the recent advancements in relation to reducing the thermal noise in switched capacitor Delta Sigma ADCs. In addition, we will address the challenges associated with breaking the Schreier FoM 192 dB performance barrier.

**Author / Presenter BIO**:

- In 2011 Spyros received the B. Sc. degree in Electronic Engineering and Education from School of Pedagogical and Technological Education, Athens, Greece, with main focus on telecommunications engineering.
- In 2015 he received the M. Sc. degree in Electronic Physics/Radioelectrology from the Physics Department of Aristotle University of Thessaloniki, Greece, with main focus on analog IC design.
- He is currently pursuing the PhD degree in Mixed-Signal IC Design from Microelectronic Circuits Centre Ireland (MCCI), in Tyndall National Institute, Cork, Ireland.
- His ongoing PhD research is on the field of Analog-to-Digital Converters (ADCs), aiming to develop new design guidelines and solutions for higher Schreier Figure-of-Merit architectures.
- He also holds the position of Research and Development Engineer at NanoXplore, Paris, France, implementing Python system-level algorithms for FPGA-based High-Speed Serial Links (HSSLs).