

**Title:** A 2nd Order 5bit hybrid CT/DT Delta-Sigma ADC implementing novel techniques for ELD compensation and coefficients trimming.

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**Abstract:** A general and well-known trend of the consumer electronics sensors market provides the increasing of accuracy together with the reduction of the power consumption in every new product generation. Further, the semiconductor shortage we are facing in this moment has stressed the already critical role played by both die-size and chip testing-time in the product definition process, representing themselves a serious limit to the industrial capability. In this context, for a given analog sensing chain the ADC is usually considered a key block whose proper choice and design can address all these aspects, resulting in a whole system optimization. In this paper, the design of a 2nd order 5bit hybrid CT/DT delta-sigma modulator is presented together with the architectural solutions used to limit the impact of the flicker noise on ADC accuracy, save current consumption, reduce testing-time and area occupation.

**Author / Presenter BIO:**

- Bachelor's degree / master's degree in electronics engineering at Politecnico di Milano in 2009 / 2012 respectively.
- Joined the MEMS sensors division of STMicroelectronics in 2012 as analog designer.
- Currently Staff Analog design engineer and Member of ST Technical Staff, focused on ADC design for low-noise and low-power MEMS sensors applications.
- Author / Co-author of several patents in the field of microelectronics for MEMS sensors and analog-to-digital conversion.