Title: Noise-Shaping SAR ADCs: from Discrete Time to Continuous Time

Author / Presenter: Hanyue Li

Organisation: Eindhoven University of Technology

Abstract: Noise-Shaping (NS) SAR ADCs become popular recently thanks to their low-power and high-resolution features. This article first summarizes and benchmarks different discrete-time (DT) NS-SAR implementations in literature. An open-loop duty-cycled residue amplifier is selected as a power-efficient solution to realize high residue gain. Then, a digital-predicted mismatch error shaping technique is introduced to improve the DAC linearity. The proposed DT NS-SAR ADC achieves 80 dB SNDR and 98 dB SFDR in a 31.25 kHz bandwidth while consuming 7.3 µW. Next, the NS-SAR architecture is extended from DT operation to continuous-time (CT) operation. The ADC sampling switch is removed and the loop filter is duty cycled to realize the CT NS-SAR operation. Compared to DT designs, the CT NS-SAR ADC is easy to drive and has an inherent anti-aliasing function. As a proof of concept, the proposed CT NS-SAR ADC achieves 77 dB SNDR and 86 dB SFDR in a 62.5 kHz bandwidth with a power consumption of 13.5 µW.

Author / Presenter BIO:

- B.Sc. degree from Zhejiang University, Hangzhou, China, in 2015
- M.Sc. degree in electrical engineering from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2016
- Currently a PhD student in the Eindhoven University of Technology
- From 2016 to 2018, he worked as an Analog Design Engineer with Qorvo, Utrecht, The Netherlands